REMARKS

Present Status of the Application

The Office Action rejected all presently-pending claims 1-16. Specifically, the Office Action rejected claims 1, 3, 4, 16 under 35 U.S.C. 102(b), as being anticipated by Jelinek et al. (US Patent 5,331,295). The Office Action also rejected claims 2, 5-15 under 35 U.S.C. 103(a) as being unpatentable over Jelinek et al. (US Patent 5,331,295) in view of Klughart (US Patent 5,798,669). The Applicant hereby respectfully requests further examination and reconsideration of those claims.

Discussion of Office Action Rejections

The Office Action rejected claims 1, 3, 4, 16 under 35 U.S.C. 102(b), as being anticipated by Jelinek et al., US Patent 5,331,295. Applicants respectfully traverse the rejections for at least the reasons set forth below.

The features are recited in claims 1. For example, independent claim 1 recited the features.

With respect to claim 1, independent claim 1 recites the features as follows:

> 1.A voltage control oscillator, for outputting a clock signal with a frequency according to an input voltage, comprising:
> ***a constant current source, for providing a reference current***;
> ***a voltage/ current converter***, *coupled to the constant current source, **for determining a first current passing through the voltage/ current converter according to the input voltage***;
> ***a current mirror***, having ***a first current terminal and a second current terminal***, the first current terminal being coupled to the constant current source, for ***determining a third current passing through the second current terminal according to the second current passing through the first current terminal,***

wherein the second current is the reference current subtracted by the first current; and

an oscillating circuit, coupled to the second current terminal of the current mirror, for determining the frequency of the outputted clock signal according to the third current. (Emphasis Added)

The present invention is directed to a voltage control oscillator. The voltage control oscillator, as shown in FIG 2A, includes a constant current source CS, a voltage/ current converter 220, a current mirror CM and an oscillating circuit 230. The constant current source CS provides a predetermined constant reference current *I*. The voltage/ current converter 220 is coupled to the constant current source CS, for determining a first current *IA* flowing through the voltage/ current converter 220 according to the input voltage VCOIN. The current mirror CM has a first current terminal coupled to the constant current source CS, for determining a third current *IC* flowing through a second current terminal according to the second current *IB* flowing through the first current terminal, wherein the second current *IB* is the reference current *I* subtracted by the first current *IA*. The oscillating circuit 230 is coupled to the second current terminal of the current mirror CM, for determining a frequency of the clocking signal CLK according to the third current *IC*. By such arrangement that third current *IC* is determined according to the second current *IB*, which is the reference current *I* subtracted by the first current *IA*, the third current *IC* and the first current *IA* caries inversely to each other, which make the VCO of the invention capable of compensating temperature variation and fabrication process fluctuation.

Jelinek et al. do not teach constant current source CS with a predetermined constant reference current *I*. As shown in Jelinek's FIG. 1, the reference current means the current for the attenuator 16 (the sum of the first split current passing through left transistor of 16 and the

second split current passing through right transistors of 16) and is obtained by subtracting the ***variable*** second current provided by the second current source 14 from the constant first current provided by the first current source 12. Thereof, Jelinek et al. disclose a ***variable*** reference current instead of the constant current CS in the invention.

Moreover, as shown in Figure 1 and 2, and as stated in col.4, line 50-col. 5, line 3 of the Jelinek reference,

> The attenuator 16 compares the input voltage on node 20 to the reference voltage on node 104 so as to vary the second split current to drive ring oscillator 22 at the desired frequency. If the input voltage on node 20 is greater than the reference voltage on node 104, more current is drawn through N-channel transistor 94 than N-channel transistor 92 and thus the second split current is larger than the first split current. As a result, more current is drawn through P-channel transistor 108 and current mirror 110 as the input voltage increases, and the amount of current mirrored into ring oscillator 22 also increases.
>
> Conversely, as the input voltage on node 20 decreases, the second split current through N-channel transistor 94 decreases and, as a result, less current is drawn through P-channel transistor 108 and current mirror 110 and the current mirrored into ring oscillator 22 decreases. Thus, once the currents of the two current sources are combined and modulated by the attenuator, the resulting current through the right branch of the attenuator tracks the current needs of the current starved inverters of ring oscillator 22.

Jelinek et al. disclose the attenuator 16 including a ***differentiation circuit*** that generates the first split current and the second split current, wherein the first split current and the second split current are obtained by ***comparing the input voltage Vfilter 20 to the reference voltage Vref.*** The attenuator 16 converts the second split current to the control current (right N-type transistors) corresponds to the ***difference*** between the input voltage ***Vfilter*** 20 and the reference voltage ***Vref.*** The current drawn through P-channel transistor 108 is controlled by the input voltage ***Vfilter*** 20 and the current at node 90 is used to limit a range

of the current drawn through P-channel transistor 108. However, in the invention, the voltage/current converter 220 as shown in FIG 2A of the present invention determines the first current *IA* according to the input voltage VCOIN without comparing to reference voltage. Furthermore, the second current *IB* in the present invention obtained by subtracting the first current *IA* from the reference current *I*.

The structure shown in Fig. 1 recited by Jelinek et al. falls short of disclosing, teaching, or even suggesting any features above-mentioned and is significantly different from that of the present invention.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1 patently defines over the prior art references, and should be allowed. For at least the same reasons, dependent claims 3, 4 and 16 patently define over the prior art as well.

Rejection under 35 U.S.C. 103(a)

The Office Action also rejected claims 2, 5-15 under 35 U.S.C. 103(a) as being unpatentable over Jelinek et al. in view of Klughart US Patent 5,798,669. Applicants respectfully traverse the rejections for at least the reasons set forth below.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a combination of references, the cited combination of references must disclose, teach, or suggest, either implicitly or explicitly, all features of the claims at issue. In view of the reasons set forth above, Jelinek et al. does not disclose, teach, or suggest all features of claim 1 and the Klughart reference dose not remedy the deficiency.

Consequently, the combination of Jelinek et al. in view of the Klughart reference does not render claims 2-15 obvious, and the rejection should be withdrawn.

Customer No.: 31561
Application No.: 10/711,380
Docket No.: 13464-US-PA

CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims 1-16 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : February 22, 2006

Respectfully submitted,

Belinda Lee

Belinda Lee
Registration No.: 46,863

Jianq Chyun Intellectual Property Office
7th Floor-1, No. 100
Roosevelt Road, Section 2
Taipei, 100
Taiwan
Tel: 011-886-2-2369-2800
Fax: 011-886-2-2369-7233
Email: belinda@jcipgroup.com.tw
Usa@jcipgroup.com.tw